DEVELOPMENT OF NEW MICROCONTROLLER BASED POWER SUPPLY CONTROL UNITS AT ELSA

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Abstract

At the electron stretcher facility ELSA electrons are accelerated with a high ramping speed of 6 GeV/s. This leads to strong requirements on the main magnets power supplies. In particular, any synchronization errors directly result in beam tune shifts and, at worst, beam loss.

The existing thirty years old control units are now being replaced by new in-house developed versatile microcontroller based ones. These allow the application of arbitrary ramp patterns and actual value acquisition in realtime. With an ethernet interface the ramp patterns can be uploaded directly to the power supplies. The flexible design also allows usage of the module to control other power supplies, e.g. those of the orbit correction magnets.

This presentation will give details on the developed hardware design and the performance of the modules compared to the existing ones.

POWER SUPPLIES AT ELSA

ELSA is a three-stage accelerator consisting of an injector with a 20 MeV LINAC, a 1.2 GeV booster synchrotron and a so-called *stretcher ring* for post acceleration to 3.2 GeV.

One acceleration cycle is typically 6 s long. Electrons from the injector stage are accumulated in the stretcher ring at 1.2 GeV and afterwards the beam energy is increased to a maximum of 3.2 GeV within 333 ms. This yields to a ramping speed of 6 GeV/s. A typical ELSA cycle is shown in Fig. 1.

Precise timing on the energy ramp imposes high requirements on the power supplies of the main magnets. The high ramp speed corresponds to a field change of 1.8 T/s of the main dipoles and thus a change in the supplied current of 5.2 kA/s. For the other magnets, e.g. quadrupoles, the slope is lower but still in the order of 1 kA/s.

In total there are six power supplies for the main magnets[1] manufactured by HOLEC . They require an analog set point value in the range from 0 V to 10 V being proportional to the desired current as well as digital signals for slow control of the device. At the moment these are provided by 30 years old in-house developed interface cards, so-called *MACS* CPUs, which are connected to VME CPUs via HDLC and finally via ethernet to the control system.

To avoid tracking errors on the ramp all interfaces are triggered by a common hardware *ramp start* trigger.

As a vital component of the accelerator these old MACS systems are now being replaced by a new microcontroller based solution. Goals for the new design are the change

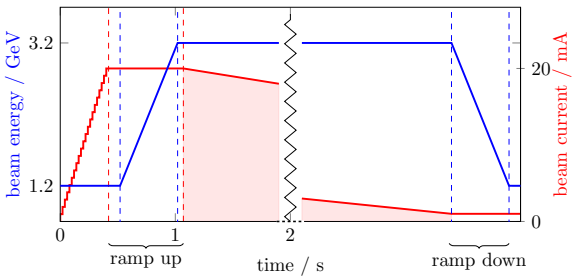

Figure 1: ELSA operation cycle consisting of accumulation, ramp up, extraction and ramp down phase.

from equidistant pre-sampled ramp patterns $I(t)$ to piecewise linear approximated ones and the ability to split the whole cycle timing into a ramp-up and ramp-down part (see Fig. 1) required for the new timing system [1].

Secondarily the new control units can be used for the corrector magnet power supplies as well [2], thus allowing to steer all magnets the same way. It also reduces tracking errors between the main magnets and the correctors on the energy ramp.

In total there are 54 corrector magnets each equipped with its own power supply. The interface is basically the same as for the main magnets except that the analog voltage is bipolar (±8 V) and the maximum current for the corrector magnets is ±8 A. Due to the high number of required power supplies it was decided to steer 4 power supplies mounted into one rack from one control unit.

HARDWARE DESIGN

Design goal for the new control units is, that all magnet power supplies can be operated with a uniform hardware module. A corresponding block diagram is shown in Fig. 2. A specialized daughter board is used to interface the different power supply's back plane connectors.

Crucial elements of the new control unit are two microcontrollers manufactured by *Atmel*. One, an *AT32UC3A1256* model is used for communication and other low priority tasks. With an attached *ethernet PHY*[2] the controller can be integrated into the existing networking infrastructure for configuration purposes and communication. Digital outputs and inputs are used for slow control of the attached power supply.

The other controller, an *ATXMEGA128A1U*, is used for real time tasks such as the output of DAC data on a regular time basis. A connected oscillator with 16 MHz and an accuracy of 30 ppm supplies the controller with a clock signal. The clock frequency is internally doubled using an

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[1] dipoles, 2 quadrupole families, 2 sextupole families and extraction sextupules

[2] Integrated circuit for the physical interface to the network.

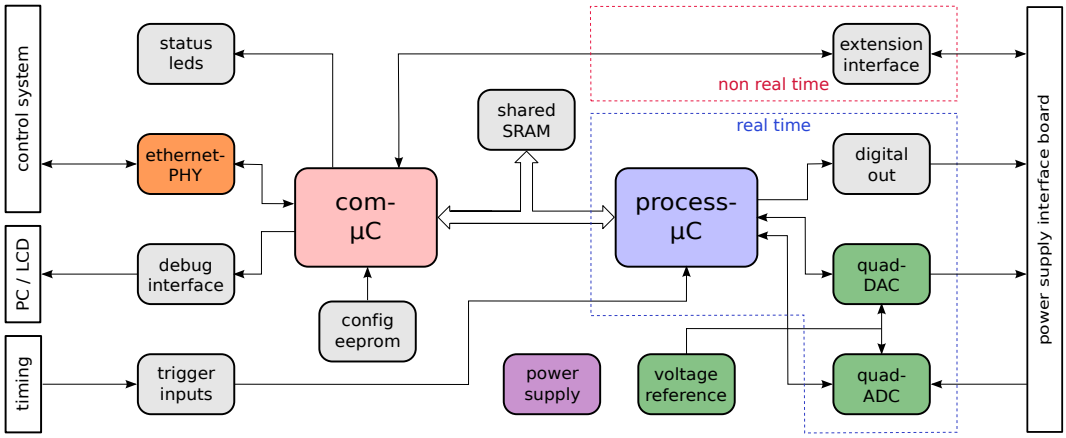

Figure 2: Block diagram of the hardware modules.

integrated PLL circuit. One digital output, also with real time capabilities, is used to switch the *bridge select*[3] of the HOLEC power supplies.

For data exchange the two microcontrollers are connected to the same 4 Mbit SRAM using an 8 bit data and 19 bit address interface. During access of one controller to the RAM (either reading or writing), access of the other controller is inhibited by a *busy line*. Access from the process controller is always prioritized.

Furthermore there is an analog stage for set point output to the power supplies. The ADC and DAC are operated with a high precision voltage reference and support up to 4 output channels. The output peak voltage ranges from −10 V to 10 V (bipolar configuration) or from 0 V to 10 V (unipolar configuration) using a resolution of 16 bit[4]. The maximum output sample rate of the ADC is 2000 samples/s.

Two isolated TTL trigger inputs allow for synchronization of the control units of the different magnet families. One trigger input is designed to start the energy ramp upwards, the other to start the ramp downwards to injection energy. Both triggers are generated by the new timing system which will be installed in the next months.

For both types of power supplies a dedicated adapter board was designed. It allows for integration of the control units into the magnet power supplies used at the accelerator facility. Both boards feature latches for digital input/output signals or status indicators (e.g. LEDs) and an 8 bit data bus connection to the communication µC . The analog signal is also routed to the backplane or to a front panel connector. The boards come in two versions, one is a double-sized euro card for the HOLEC power supplies, and the other an euro card for the corrector magnet power supplies.

Furthermore a debug interface can be connected to the microcontroller (µC) board. This connection can be used for in-field debugging of the device using a development board (with integrated dot matrix display) or for connecting a PC using a serial RS232 interface.

[3] The power supply has two bridge circuits. One for slopes ≤ 1 GeV/s with low ripple, and one for slopes ≥ 1 GeV/s.

[4] precision of 1.5 LSB INL

SOFTWARE DESIGN

The microcontrollers are programmed using the high level programming language C. Both programs have a common code base to ease communication through the SRAM. For communication using the network protocols TCP and UDP the third party *TCP/IP* stack called *lwIP*[5] is used.

The shared SRAM, which is attached to both microcontrollers is divided into 5 partitions. The layout is shown in Fig. 3. The smallest ones are used for *online configuration*, *control registers* of the process microcontroller and *status registers*. The online configuration is downloaded upon reset of the communication microcontroller from the accelerator's control system via ethernet. The dataset contains basic parameters, like the number of channels used, the maximum voltage slope, maximum output voltage and other absolute maximum ratings. Also the sampling rate, either for the DAC or the ADC, can be configured[6]. With this approach the control units are independent of the power supplies to be controlled and can be replaced easily.

The control unit can be operated in two different modes, which can be set in the *control register*. In *triggered ramp mode* it reacts on an incoming trigger and plays back the pre-programmed ramp. Or, it can be configured to ignore all trigger inputs and set the output voltage to a static set point stored in the SRAM. In both cases the actual state (e.g. "ramping", "end of ramp reached") is stored in the SRAM in the *status registers*.

The fourth partition is used by the process microcontroller for storage of digitized analog data, which represents the actual current output of the power supply. The sampling of the ADC is synchronously started with the ramp playback. At regular time intervals the communication µC checks for new data indicated by a bit which is set by the process µC . It then reads out the changed data from the memory block and sends it via ethernet to the control system for display.

[5] lightweight IP

[6] The default sampling rate is 100 kHz for the DAC and 1 kHz for the ADC.

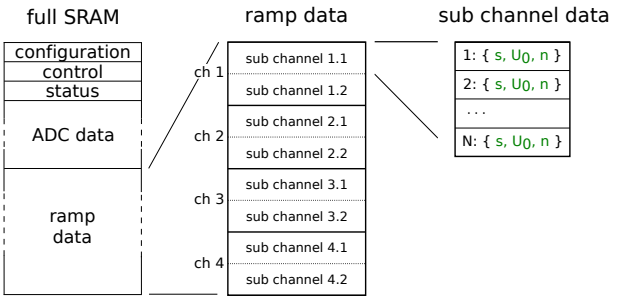

Figure 3: Partitions of the shared SRAM.

The ramp data occupies largest part of the SRAM. The whole block is partitioned as follows:

$$2 \text{ data sets} \times 4 \text{ channels} \times 2 \text{ subchannels} \quad ,$$

where the data sets are used to allow for uploading new ramp data to an inactive segment without disturbing the actual playback. The active data set can be chosen by the control system. The channels refer to the four different output channels in case of the corrector magnet power supplies (4 per control unit). Furthermore the subchannels are used for storage of the two parts (ramp up and ramp down) of the cycle.

The ramp data itself is stored as piecewise linear functions. These are parametrized by their offset U_0, their slope s and the number n of equidistant sampling points. The time interval between the sampling points can be configured (via the *configuration registers*) and is typically set to 10 µs.

To fulfill the strict real time constraints, the playback is internally managed using timer interrupts within the microcontroller. This results in a worst case timing jitter of 94 ns.

Control System Integration

The ELSA control system is responsible for calculation of the ramp data (see Fig. 4). For the main dipole magnets this is done as follows: The linear energy ramp $E(t)$ is translated to the corresponding magnetic field $B(t)$. Furthermore the saturation effects in the ferromagnetic dipole magnets have to be taken into account while converting the field strength to the appropriate current. Because this effect is non-linear, it has to be approximated by the already mentioned piecewise linear functions (see Fig. 5). Slope s, offset U_0 and number of steps N for each linear function are well chosen to have a maximum deviation of one LSB of the 16 bit DAC.

STATUS AND OUTLOOK

The microcontroller board is almost ready for production use. All offline tests (without an attached power supply) have been successfully passed. The design of the adapter boards for the two different types of power supplies is currently under review and will be tested in May 2015. Also the in-field tests will start this May.

The performance looks very promising to improve the tracking errors by the main power supplies. Furthermore it is

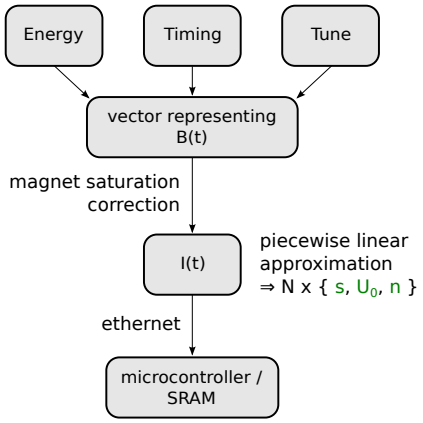

Figure 4: Calculation of ramp data.

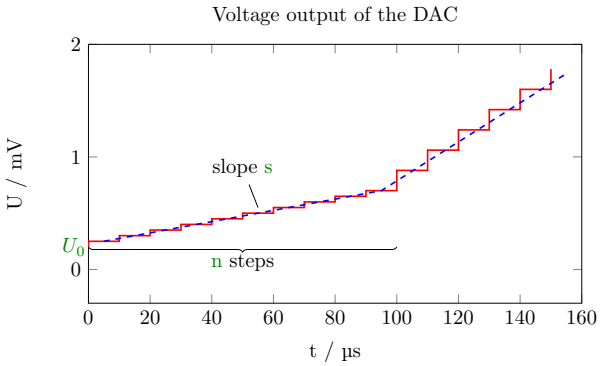

Figure 5: Piecewise linear approximation (shown in dashed blue) of the desired non-linear function for $I(t)$, represented by $U(t)$ (shown in red).

a crucial component for the upcoming upgrade of the timing system because the old modules do not support varying cycle durations.

After installation the performance has to be verified. This will be done by an energy calibration using resonant spin depolarization techniques [3] with an accuracy of 1×10^{-4} GeV.

REFERENCES

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